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EDUCATION

Institution	Concentration	Degree/Date
The University of Minnesota, Minneapolis	EE	Ph.D., 1989
The University of Iowa, Iowa City	EE	M.S., 1986
National Taiwan University, Taipei, Taiwan	EE	B.S., 1981

ACADEMIC EXPERIENCE

Institution/Organization	Position	Dates
Wright State University, Dayton, Ohio	Professor	2000-present
Wright State University, Dayton, Ohio	Associate Professor	1995-2000
Wright State University, Dayton, Ohio	Assistant Professor	1989-1995

RESEARCH INTERESTS

VLSI/FPGA design, spanning digital designs and RF components and extending to embedded system applications, such as radar and ultra-wideband digital receivers.

PROFESSIONAL SERVICE

Editorial Board	Service
Integration, the VLSI Journal	Associate Editor (2010-present)
Journal of Electrical and Computer Engineering	Editor (2018-present)
VLSI Design	Editor (2009-2018)
Journal of Computers	Editor (2009-2016)
International Journal of Advancements in Computing Technology	Associate Editor-in-Chief (2009-2016)
VLSI Design	Guest Editor (2002)

Professional Committee	Service
2020 International Conference on Pervasive and Parallel Computing, Communication and Sensors (PECCS'2020)	Program Committee
2020 The International Conference on Computer Systems and Communication Technology (ICCSCT'2020)	Program Committee
2019 International Conference on Pervasive and Embedded Computing and	Program Committee

Communication Systems (PECC'2019)	
2018 International Conference on Pervasive and Embedded Computing (PEC'2018)	Program Committee
2017 International Conference on Ambient Systems, Networks, Technologies	Program Committee
2017 International Conference on Pervasive and Embedded Computing (PEC'2017)	Program Committee
2016 IEEE International Instrumentation and Measurement Technology Conf. (I^2MTC'2016)	Technical Committee
2016 International Conference on Pervasive and Embedded Computing (PEC'2016)	Program Committee
2015 IEEE International Instrumentation and Measurement Technology Conf. (I^2MTC'2015)	Technical Committee
2015 International Conference on Smart Sensors and Application	Technical Committee
2015 IEEE International Workshop on the Design and Performance of Networks on Chip	Technical Committee
2014 IEEE International Instrumentation and Measurement Technology Conf. (I^2MTC'2014)	Technical Committee
2013 IEEE International Instrumentation and Measurement Technology Conf. (I^2MTC'2013)	Technical Committee
2013 IEEE International Conference on Smart Instrumentation, Measurement and Applications (ICSIMA'2013)	Technical Committee
2012 IEEE International Instrumentation and Measurement Technology Conf. (I^2MTC'2012)	Technical Committee
2011 IEEE International Instrumentation and Measurement Technology Conf. (I^2MTC'2011)	Technical Committee
2010 IEEE International Symposium on Circuits and Systems (ISCAS'2010)	Review Committee for "Ckts and Sys for Comm"
2010 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS'2010)	Technical Committee
2009 IEEE International Symposium on Circuits and Systems (ISCAS'2009)	Review Committee for "Ckts and Sys for Comm"
2008 IEEE International Midwest Symposium on Circuits and Systems	Review Committee
2008 IEEE International Instrumentation and Measurement Technology Conf. (I^2MTC'2008)	Technical Committee
2008 IEEE International Symposium on Circuits and Systems (ISCAS'2008)	Review Committee for "Ckts and Sys for Comm"
2007 IEEE International Symposium on Circuits and Systems (ISCAS'2007)	Review Committee for "Ckts and Sys for Comm"
2007 IEEE International Midwest Symposium on Circuits and Systems	Review Committee
2006 IEEE Instrumentation and Measurement Technology Conf. (IMTC'2006)	Technical Committee
2006 IEEE International Symposium on Circuits and Systems (ISCAS'2006)	Review Committee for "Ckts and Sys for Comm"
2005 IEEE Instrumentation and Measurement Technology Conf. (IMTC'2005)	Technical Committee
2004 IEEE Instrumentation and Measurement Technology Conf. (IMTC'2004)	Technical Committee
2003 Annual Conference of the IEEE Industrial Electronics (IECON'2003)	Technical Committee
2002 IEEE International ASIC/SOC Conference (SOCC'2002)	Technical Committee
2001 IEEE International ASIC/SOC Conference (SOCC'2001)	Technical Committee
2000 IEEE International ASIC/SOC Conference (SOCC'2000)	Technical Committee
1996 IEEE International ASIC Conference and Exhibit (ASIC'1996)	Technical Committee
1995 Ohio Symposium on Information Science and Technology	Program Committee
1995 IEEE International ASIC Conference and Exhibit (ASIC'1995)	Technical Committee

Journal and Conference	**Service**
1995 the 6th VLSI Design/CAD Symposium	Plenary Speaker
IEEE Transactions on Computer-Aided Design	Technical Reviewer
IEEE Transactions on Computers	Technical Reviewer
IEEE Transactions on Reliability	Technical Reviewer
IEEE Transactions on Aerospace & Electronic Systems	Technical Reviewer
IEEE Transactions on Circuits and Systems (I), (II)	Technical Reviewer
IEEE Transactions on Instrumentation and Measurement	Technical Reviewer

IEEE Transactions on VLSI Systems	Technical Reviewer
IEEE Transactions on Semiconductor Manufacturing	Technical Reviewer
IEEE Transactions on Aerospace and Electronic Systems	Technical Reviewer
IEEE Signal Processing Letters	Technical Reviewer
ACM Transactions on Embedded Computing Systems	Technical Reviewer
International Journal of Computer Aided VLSI Design	Technical Reviewer
VLSI Design Journal	Technical Reviewer
Journal of Computers	Technical Reviewer
International Journal of Advancements in Computing Technology	Technical Reviewer
VLSI Design: An International Journal	Technical Reviewer
Journal of Electronic Testing	Technical Reviewer
ACM Transactions on Embedded Computing Systems	Technical Reviewer
Journal of VLSI Signal Processing Systems	Technical Reviewer
ACM/IEEE Design Automation Conference (DAC)	Technical Reviewer
IEEE International Conference on Computer-Aided Design (ICCAD)	Technical Reviewer
IEEE International Symposium on Circuits and Systems (ISCAS)	Technical Reviewer
IEEE International Midwest Symposium on Circuits and System (IMSCAS)	Technical Reviewer
IEEE Instrumentation and Measurement Technology Conf. (IMTC)	Technical Reviewer
IEEE International ASIC/SOC Conference	Technical Reviewer
International Test Conference (ITC)	Technical Reviewer
VLSI Test Symposium (VTS)	Technical Reviewer

SCHOLARSHIP

Book and Chapters

1. Chen, C.-I. H., Timing Analysis and Optimization for DSM IC, Special Issue, *VLSI Design Journal*, 2002.
2. Chen, C.-I. H. and Kumar, A., BiCMOS Logic Circuits, the Wiley Encyclopedia of Electrical and Electronics engineering, edited by Webster, J. G., John Wiley and Sons Inc., pp. 279-293, 1999.

Peer-Reviewed Journal Articles and Papers Published in Full in Conference Proceedings

3. Abdulhamed, B. and Chen, C.-I. H., "High Sensitivity Digital Instantaneous Frequency Measurement Receiver for Precise Frequency Analysis," accepted for publication in ***Journal of Computer and Communications.***
4. Jayarama, K. and Chen, C.-I. H., "Enhanced Wideband Frequency Estimation via FFT: Leveraging Polynomial Interpolation and Array Indexing," ***Journal of Computer and Communications***, Vol. 12. No. 1, pp. 35-48, Jan., 2024.
5. Wang, Y., Ren, J. and Chen, C.-I. H., "Calibration of Optimized Minimum Inductor Bandpass Filter with Controllable Bandwidth and Stopband Rejection," ***Integration, the VLSI Journal***, Vol. 81, pp. 300-321, July 2021.
6. Allwin, P. S. and Chen, C.-I. H., "A Low-Area, Low-Power Dynamically Reconfigurable 64-bit Media Signal Processing Adder," ***Journal of Computer and Communications***, Vol. 9, No. 3, pp. 54-69, March 2021.
7. Daram, P. and Chen, C.-I. H., "Smart FFT Measurement for Reconfigurable Sensors Using a Wideband Digital Receiver," *IEEE National Aerospace and Electronics Conference*, pp. 200-203, 2021.
8. Liu, F. and Chen, C.-I. H., "High Two-Signal Dynamic Range and Accurate Frequency Measurement for Close Frequency Separation Wideband Digital Receiver Using Adaptive Gain Control and Dynamic Thresholding," ***Integration, the VLSI Journal***, Vol. 72, pp. 72-81, May 2020.
9. Wang, Y., Chen, J. and Chen, C.-I. H., "Chebyshev Bandpass Filter Using Resonator of Tunable Active Capacitor and Inductor, ***VLSI Design***, Vol. 2017, Article ID 5369167, 12 pages, May 2017.
10. Lin, E., Chen, C.-I. H., Liou, L. L. and Lin, D. M., "Performance Analysis of Digital Wideband Receiver based on Reconstruction of Compressive Sensing Data," *IEEE Radar Conference*, pp. 0830-0835, Seattle, WA, May 2017.
11. Benson, S. and Chen, C.-I. H., Lin, M. D. and Liou, L. L., "High Linear Chirp Receiver Using High Resolution Time-of-Arrival Estimation," ***IEEE Transactions on Aerospace and Electronic Systems***, Vol. 52, No. 3. pp. 1146-1154, June 2016.

12. Xue, H. and Chen, C.-I. H., "Timing and Power Optimization Using Mixed-Dynamic-Static CMOS," ***International Journal of Emerging Technology and Advanced Engineering***, Vol. 6, No. 3, pp. 19-28, November 2016.
13. Lin, E., Chen, C.-I. H., Liou, L. L. and Lin, D. M., "Detection and Sensitivity Analysis of Compressed Sensing Electronic RF Receiver," *IEEE Radar Conference*, pp. 1-6, Philadelphia PA, May 2016.
14. Chen, J. and Chen, C.-I. H., "Process Variation Aware Wide Tuning Band Pass Filter for Steep Roll-Off High Rejection," ***VLSI Design***, Vol. 2015, Article ID 408035, pp. 1-9, 2015.
15. George, K. and Chen, C.-I. H., "Performance Measurement of a High-Performance Computing System Utilized for Electronic Medical Record Management," ***International Journal of Advancements in Computing Technology***, Vol. 7, No. 1, pp. 1-8, January 2015.
16. Chen, J. and Chen, C.-I. H, "1-2 GHz Tuning Frequency Band Pass Filter with Controllable Pass Band and High Stopband Rejection, *IEEE International Microwave Symposium*, pp. 1-4, Phoenix, AZ, May 2015.
17. George, K. and Chen, C.-I. H., "Multiple Signal Detection Digital Wideband Receiver Utilizing Hardware Accelerators," ***IEEE Transactions on Aerospace and Electronic Systems***, Vol. 49, No. 2, pp. 706-715, April 2013.
18. George, K. and Chen, C.-I. H., "Measurement Setup and Performance Analysis of Digital Receiver System with Multiple Signal Detection and Expandable Bandwidth Capabilities on a Multi-Processor Hardware Platform," ***International Journal of Engineering Sci. and Man.***, Vol. 3, No. 1, pp. 46-54, 2013.
19. George, K. and Chen, C.-I. H., "Modular Test RF Instrumentation and Measurement for a Hybrid Computing Digital Wideband Receiver," *IEEE International Instrumentation and Measurement Technology Conference*, pp. 352-356, May 2014.
20. Boppana, V. K., S. Ren and Chen, C.-I. H., "Low Power and High Speed CPL-CSA Adder," *2014 IEEE National Aerospace and Electronics Conference,* Dayton, OH, July 2014.
21. Liou, L. L., Lin, M. D., Lin, E. and Chen, C.-I. H., "Sensitivity Simulation of Compressed Sensing Based EW Receiver Using Orthogonal Matching Pursuit Algorithm," *IEEE National Aerospace and Electronics Conference*, pp. 89-94, Dayton, OH, July 2014.
22. Yelamarthi, Y. and Chen, C.-I. H., "Timing Optimization and Noise Tolerance for Dynamic CMOS Susceptible to Process Variations," ***IEEE Transactions on Semiconductor Manufacturing***, Vol. 25, No. 2*,* pp. 255-265, May 2012.
23. George, K. and Chen, C.-I. H., "A Hybrid Computing Platform Digital Wideband Receiver Design Instrumentation and Performance Measurement," ***IEEE Transactions on Instrumentation and Measurement,*** Vol. 60, No. 12*,* pp. 3956-3958, Dec. 2011.
24. George, K. and Chen, C.-I. H., "Biologically-Inspired Signal Processor Using Lateral Inhibition and Integrative Function Mechanisms for High Instantaneous Dynamic Range," ***International Journal on Smart Sensing and Intelligent Systems,*** Vol. 4, No. 4*,* pp. 547-567, Dec. 2011.
25. Benson, S. and Chen, C.-I. H., "Adaptive Thresholding for High Dual-Tone Signal Instantaneous Dynamic Range in Digital Wideband Receiver," ***IEEE Transactions on Instrumentation and Measurement***, Vol. 60, No. 5, pp. 1869-1875, May 2011.
26. George, K. and Chen, C.-I. H., "Automated Mixed-Signal SoC BIST Synthesis utilizing Hardware Accelerators," *IEEE International Instrumentation and Measurement Technology Conference*, May 2012.
27. Lin, M. D., Liou, L. L., Benson, S. and Chen, C.-I. H., "Mono-bit Digital Chirp Receiver using mono-bit IFM (Instantaneous Frequency Measurement) Receiver as a core", *2011 IEEE National Aerospace and Electronics Conference*, Dayton, OH, July 2011.
28. Yelamarthi, Y. and Chen, C.-I. H., "A Timing Optimization Technique for Nanoscale CMOS Circuits Susceptible to Process Variations," *IEEE International Instrumentation and Measurement Technology Conference,* pp. 109-113, Hangzhou, China, May 2011.
29. George, K. and Chen, C.-I. H., "Design and Performance Evaluation of a Digital Wideband Receiver on a Hybrid Computing Platform," *IEEE International Instrumentation and Measurement Technology Conference,* Hangzhou, China, May 2011.

30. Yelamarthi, Y. and Chen, C.-I. H., "Delay Optimization Considering Power Saving in Dynamic CMOS Circuits," *IEEE/ACM International Symposium on Quality Electronic Design,* pp. 364-369, Santa Clara, CA, March 2011.

31. Yelamarthi, Y. and Chen, C.-I. H., "Dynamic CMOS Load Balancing and Path Oriented In Time Optimization Algorithms to Minimize Delay Uncertainties from Process Variations," ***VLSI Design***, Vol. 2010, Article ID 230783, pp. 1-13, 2010.

32. Lee, Y.-H. G. and Chen, C.-I. H., "Dynamic Kernel Function Fast Fourier Transform with Variable Truncation Scheme for Wideband Coarse Frequency Detection," ***IEEE Transactions on Instrumentation and Measurement,*** Vol. 58, No. 5, pp. 1495-1504, May 2009.

33. George, K. and Chen, C.-I. H., "Logic Built-In Self-Test for Core-Based Designs on System-on-a-Chip," ***IEEE Transactions on Instrumentation and Measurement,*** Vol. 58, No. 5, pp. 1555-1562, May 2009.

34. Yelamarthi, Y. and Chen, C.-I. H., "Process-Variation Aware Timing Optimization for Dynamic and Mixed-Static-Dynamic CMOS Logic," ***IEEE Transactions on Semiconductor Manufacturing***, Vol. 22, No, 1, pp. 31-39, 2009.

35. Benson, S. and Chen, C.-I. H., "Adaptive Thresholding for High Dual-Tone Signal Instantaneous Dynamic Range in Digital Wideband Receiver," *IEEE International Instrumentation and Measurement Technology Conference*, pp. 616-619, Austin, Texas, May 2010.

36. Lee, Y.-H. G. and Chen, C.-I. H., "Fixed-Point Fixed-Precision Dynamic Kernel Function FFT Processor for Wideband Signal Detection," *IEEE International Instrumentation and Measurement Technology Conference*, pp. 397-401, Austin, Texas, May 2010.

37. Lee, Y.-H. G. and Chen, C.-I. H., "Bit-Precision and Performance Analysis of Dynamic Kernel Function Fast Fourier Transform," *IEEE International Instrumentation and Measurement Technology Conference*, pp. 187-191, Austin, Texas, May 2010.

38. Lee, Y.-H. G. and Chen, C.-I. H., "Dual Thresholding for Digital Wideband Receivers with Variable Truncation Scheme", *IEEE International Symposium on Circuits and Systems*, pp. 920-923, Taipei, Taiwan, May 2009.

39. Zhang X.; Chen, C.-I. H. and Chakravarthy A., "Structure Design and Optimization of 2D LFSRs Based Multisequence Test Generator in Built-In Self-Test," ***IEEE Transactions on Instrumentation and Measurement***, Vol. 57, No. 3, pp. 651-663, March 2008.

40. Yelamarthi, Y. and Chen, C.-I. H., "Process Variation Aware Transistor Sizing for Load Balance of Multiple Paths in Dynamic CMOS for Timing Optimization," ***Journal of Computers,*** Academy Publisher, Vol. 3, No. 2, pp. 21-28, Feb. 2008.

41. Wibbenmeyer, J. and Chen, C.-I. H., "Built-In Self-Test for Low-Voltage High-Speed Analog-to-Digital Converters," ***IEEE Transactions on Instrumentation and Measurement***, Vol. 56, No. 6, pp. 2748-2756*,* Dec. 2007.

42. Wang, M.; Chen, C.-I. H. and Radhakrishnan, S, "Low-Power 4-b 2.5 GSPS Pipelined Flash Analog-to-Digital Converters in 130-nm CMOS," ***IEEE Transactions on Instrumentation and Measurement,*** Vol. 56, No. 3, pp. 1064-1073*,* June 2007.

43. George, K.; Chen, C.-I. H., and Tsui, J. B.-Y., "Extension of Two-Signal Spurious-Free Dynamic Range of Wideband Digital Receiver using Kaiser Window and Compensation Method," ***IEEE Transactions on Microwave Theory and Techniques****,* Vol. 55, No. 4, pp. 788-794, April 2007.

44. Yelamarthi, Y. and Chen, C.-I. H., "A Path Oriented in Time Optimization Flow for Mixed-Static-Dynamic CMOS Logic," *IEEE Midwest Symposium on Circuits and Systems*, pp. 454-457, Knoxville, Tennessee, August 2008.

45. Lee, Y.-H. G.; Helton, J. and Chen, C.-I. H., "Real-Time FPGA-Based Implementation of Digital Instantaneous Frequency Measurement Receiver," *IEEE International Symposium on Circuits and Systems,* pp. 2494-2497, Seattle, Washington, May 2008.

46. George, K. and Chen, C.-I. H., "Logic Built-In Self-Test for Core-Based Designs on System-on-a-Chip," *IEEE International Instrumentation and Measurement Technology Conference*, pp. 1503-1508, Vancouver, British Columbia, Canada, May 2008.

47. Lee, Y.-H. G.; Sarathy, V. and Chen, C.-I. H., "Dynamic Kernel Function Fast Fourier Transform with Variable Truncation Scheme for Wideband Signal Detection," *IEEE International Instrumentation and Measurement Technology Conference*, pp. 1354-1359, Vancouver, British Columbia, Canada, May 2008.

48. Keerthi, R. and Chen, C.-I. H., "Stability and Static Noise Margin Analysis of Low-Power SRAM," *IEEE International Instrumentation and Measurement Technology Conference*, pp. 1681-1684, Vancouver, British Columbia, Canada, May 2008.

49. Helton, J.; Chen, C.-I. H.; Lin, D. M. and Tsui, J. B.-Y, "FPGA-Based 1.2 GHz Bandwidth Digital Instantaneous Frequency Measurement Receiver," *IEEE/ACM International Symposium on Quality Electronic Design*, pp. 568-571, San Jose, March 2008.

50. Yelamarthi, Y. and Chen, C.-I. H., "Process Variation Aware Timing Optimization through Transistor Sizing in Dynamic CMOS Logic," *IEEE/ACM International Symposium on Quality Electronic Design*, pp. 143-147, San Jose, March 2008.

51. Wang, M. and Chen, C.-I. H., "Low-Power 1.25-GHz Signal Bandwidth 4-BIT CMOS Analog-to-Digital Converter for High Spurious-Free Dynamic Range Wideband Communications," *IEEE International SOC Conference,* pp. 109-112, Hsinchu, Taiwan, Sept. 2007.

52. Wang, M. and Chen, C.-I. H., "A High Spurious-Free Dynamic Range 4-bit ADC with Nyquist Signal Bandwidth for Wideband Communications," *IEEE International Instrumentation and Measurement Technology Conference*, (#7608) pp. 1-6, Warsaw, Poland, May 2007.

53. George, K. and Chen, C.-I. H., "Multiple Signal Detection and Measurement Using a Configurable Wideband Digital Receiver," *IEEE International Instrumentation and Measurement Technology Conference*, (#7638) pp.1-5, Warsaw, Poland, May 2007.

54. George, K. and Chen, C.-I. H., "Configurable and Expandable FFT Processor for Wideband Communications," *IEEE International Instrumentation and Measurement Technology Conference*, (#7633) pp.1-6, Warsaw, Poland, May 2007.

55. Yelamarthi, Y. and Chen, C.-I. H., "Transistor Sizing for Load Balance of Multiple Paths in Dynamic CMOS for Timing Optimization," *IEEE/ACM International Symposium on Quality Electronic Design*, pp. 426-431, San Jose, March 2007.

56. Chen, C.-I. H.; George, K.; McCormick W; Tsui, J. B. Y.; Hary S. and Graves K., "Design and Performance Evaluation of 2.5 GSPS Digital Receiver," ***IEEE Transactions on Instrumentation and Measurement****,* Vol. 54, No. 3, pp. 1089-1099, June 2005.

57. Kakulavarapu, S.; Yelamarthi, Y and Chen, C.-I. H., "Signed Multiplier Using Baugh-Wooley and On-The-Fly Conversion Algorithms," *2006 IEEE International Conference on Computers and Devices for Communications*, Kolkata, India, Dec. 2006.

58. Yelamarthi Y. and Chen, C.-I. H., "A Sub-Nanosecond High-Performance 64-bit Binary Adder," *2006 IEEE International Conference on Computers and Devices for Communications*, Kolkata, India, Dec. 2006.

59. George, K.; Chen, C.-I. H., and Tsui, J. B.-Y., "Extension of Two Signal Dynamic Range of Wideband Digital Receiver using Kaiser Window and Compensation Method," *IEEE International Microwave Symposium*, pp. 1955-1958, San Francisco, California, June 2006.

60. Chandrasekhar, V.; Chen, C.-I. H. and Yelamarthi Y., "Low-Cost Low-Power Self-Test Design and Verification for On-Chip ADC in System-on-a-Chip Applications" *IEEE International Instrumentation and Measurement Technology Conference*, pp. 1301-1306, Sorrento, Italy, April 2006.

61. Sajabi, C.; Chen, C.-I. H.; Lin D. M. and Tsui, J. B. Y., "FPGA Frequency Domain Based GPS Coarse Acquisition Processor Using FFT" *IEEE International Instrumentation and Measurement Technology Conference*, pp. 2353-2358, Sorrento, Italy, April 2006.

62. Wang, M. and Chen, C.-I. H., "Architecture and Design Synthesis of 2.5 Gsamples/s 4-b Pipelined Flash ADC in SoC Applications," *31 Annual International Conference of the IEEE Industrial Electronics*, pp. 2224-2230, Raleigh, North Carolina, November 2005.

63. Wibbenmeyer, J. and Chen, C.-I. H., "Built-In Self-Test for Analog-to-Digital Converters in SoC Applications," *31 Annual International Conference of the IEEE Industrial Electronics*, pp. 2231-2236, Raleigh, North Carolina, November, 2005.

64. Radhakrishnan, S.; Wang, M. and Chen, C.-I. H., "A Low-Power 4-b 2.5 Gsample/s Pipelined Flash Analog-to-Digital Converter Using QV Comparator and DCVSPG Encoder," *IEEE International Symposium on Circuits and Systems,* pp. 6142-6145, Kobe, Japan, May, 2005.

65. Wibbenmeyer, J. and Chen, C.-I. H., “A New Architecture of Built-In Self-Test for Analog-to-Digital Converters,” *IEEE International Instrumentation and Measurement Technology Conference*, pp. 184-189, Ottawa, Ontario, Canada, May 2005.

66. Wang, M. and Chen, C.-I. H., “Design Synthesis and Performance Measurement of Pipelined Flash ADC for SoC Applications,” *IEEE International Instrumentation and Measurement Technology Conference*, pp. 19-24, Ottawa, Ontario, Canada, May 2005.

67. Schindel, D. T. and Chen, C.-I. H., “Multiple Clipping for Optimization of Arc Draw on Active Matrix Liquid Crystal Display,” *IEEE International Instrumentation and Measurement Technology Conference*, pp. 797-802, Ottawa, Ontario, Canada, May 2005.

68. Radhakrishnan, S; Wang, M. and Chen, C.-I. H., “Low-Power 4-b 2.5 GSPS Pipelined Flash Analog-to-Digital Converters in 0.13 µm CMOS” *IEEE International Instrumentation and Measurement Technology Conference*, pp. 287-292, Ottawa, Ontario, Canada, May 2005.

69. Chen, C.-I. H. and George, K., “Configurable Two-dimensional Linear Feedback Shifter Registers for Parallel and Serial Built-In Self-Test,” ***IEEE Transactions on Instrumentation and Measurement****,* Vol. 53, No. 4, pp. 1005-1014, August 2004.

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74. Chen, C.-I. H. and George, K., “Design and Measurement of 2.5 GSPS Digital Receiver,” *2003 IEEE International Instrumentation and Measurement Technology Conference,* pp. 258-263, Colorado, May 2003.

75. Chen, C.-I. H. and George, K., “Automated Synthesis of Configurable Two-dimensional Linear Feedback Shifter Registers for Random/Embedded Test Patterns,” *IEEE/ACM International Symposium on Quality Electronic Design*, pp. 111-116, San Jose, March 2003.

76. Lin, I. and Chen, C.-I. H, “Timing Challenges for Very Deep Sub-Micron (VDSM) IC,” ***VLSI Design***, Vol. 15, No. 3, pp. 557-562, 2002.

77. Huang, J. A. and Chen, C.-I. H. , “Timing-Driven Testable Convergent Tree Adders,” ***VLSI Design***, Vol. 15, No. 3, pp. 637-645, 2002.

78. Chen, C.-I. H., "Timing Analysis and Optimization for DSM IC - Editorial," ***VLSI Design***, Vol. 15, No. 3, pp. 555-556, 2002

79. Chen, C.-I. H. and Wagh, M. “Testability Synthesis for Jumping Carry Adders,” ***VLSI Design***, Vol. 14, No. 2, pp. 155-169, 2002.

80. Chen, C.-I. H., “Configurable Linear Feedback Shifter Registers for Random/Embedded Test Patterns,” a poster session paper in 5th *IEEE International ASIC/SOC Conference,* September 2002*.*

81. Chen, C.-I. H., “Synthesis for Configurable Linear Feedback Shifter Registers for Detecting Random-Pattern-Resistant Faults," *IEEE/ACM 14th International Symposium on System Synthesis*, pp. 203-208, September 2001.

82. Chen, C.-I. H. and Zhou, Y., “Configurable 2-D Linear Feedback Shifter Register for Built-In Self-Test Designs,” ***VLSI Design****,* Vol. 11, No. 2, pp. 149-159, 2000*.*

83. Wagh, M. and Chen, C.-I. H., “Testability Synthesis for 32-Bit Jumping Carry Adders*,” the IEE International ASIC/SOC*, Rochester, NY, pp. 130-134, September 1999.

84. Wagh, M. and Chen, C.-I. H., "High-Level Design Synthesis with Redundancy Removal for High Speed Testable Adders, *IEEE International Symposium on Circuits and Systems*, Orlando, FL, June 1999.

85. Hamid, M. E. and Chen, C.-I. H., "A Note to Low Power Linear Feedback Shift Registers," ***IEEE Transactions on Circuits and Systems***, Part II, Vol. 45, No. 9, pp. 1304-1307, September 1998.

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92. Pok, S.; Chen, C.-I. H.; Schamus, J.; Montgomery C. T. and Tsui, J. B. Y., "ASIC for 1-GHz Wide Band Monobit Receiver," *IEEE International Symposium on Circuits and Systems*, MPA 6-4, Monterey, CA, June 1998.

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100. Chen, C.-I. H. and Noh, T., "A Novel Approach to VHDL Behavioral ATPG/Fault Simulation," *the 1995 IEEE International Conference on Signal Processing, Circuits and Systems,* Singapore, pp. 225-230, July 1995.

101. Chen, C.-I. H. and Yuen, J., "Automated Synthesis of Pseudo-Exhaustive Test Generator in VLSI BIST Design," ***IEEE Transactions on VLSI Systems,*** Vol. 2, No. 3, pp. 273-291, September 1994.

102. Chen, C.-I. H. and Kumar, A., "Comments on Area-Time Optimal Adder Design," ***IEEE Transactions on Computers***, Vol. 43, No. 4, pp. 507-512, April 1994.

103. Chen, C.-I. H., etc. "Task Allocation and Reallocation for Fault Tolerance in Multicomputer Systems, ***IEEE Transactions on Aerospace and Electronic Systems***, Vol. 30, No. 4, pp. 1094-1104, October 1994.

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107. Chen, C.-I. H. and Kumar, A., "Area-Time Optimal Digital BiCMOS Carry Look-Ahead Adder," *the IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS*), Taipei, Taiwan, pp. 115-120, December 1994

108. Chen, C.-I. H.; O'Bleness, F.; Yuen, J. and Chan, C.-L., "An Efficient Approach to Low Cost Sequential Circuit Testing in a BIST Environment," *the IEEE International Application Specific Integrated Circuit (ASIC) Conference and Exhibit*, Rochester, NY, pp. 403-406, September 1994.

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112. Chen, C.-I. H., "Circuit Partitioning for Pseudo-Exhaustive Test," *the IEEE International Application Specific Integrated Circuit (ASIC) Conference and Exhibit*, Rochester, NY, pp. 152-155, September 1993.

113. Chen, C.-I. H. etc., "Redundant Task-Allocation in Multicomputer Systems," ***IEEE Transactions on Reliability***, Vol. 41, No. 3, pp. 336-342, September 1992.

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115. Chen, C.-I. H. and Yuen, J., "Concurrent Test Scheduling in VLSI BIST Environment," *the IEEE International Conference on Computer Design (ICCD*), Boston, MA, pp. 256-259, October 1992.

116. Chen, C.-I. H. and Yuen, J., "An Efficient Approach to Pipeline Scheme for Concurrent Testing of VLSI Circuits," *the IEEE International Symposium on Circuits and Systems (ISCAS),* San Diego, CA, pp. 657-660, May 1992.

117. Yuen, J.; Chen, C.-I. H. and Siferd, R., "VLSI Design and Implementation of Self-Testing Systolic Array Chip for Signal Processing," *the IEEE International Symposium on Circuits and Systems (ISCAS),* San Diego, CA, pp. 375-378, May 1992.

118. Chen, C.-I. H., "BISTSYN - A Built-In Self-Test Synthesizer," *the IEEE International Conference on Computer-Aided Design (ICCAD),* San Jose, CA, pp. 240-243, November 1991.

119. Chen, C.-I. H., "Allocation of Multiport Memory with Ports of Different Type Register Transfer Level Synthesis," *the IEEE International Conference on Computer Design (ICCD*), Boston, MA, pp. 418-421, October 1991.

120. Chen, C.-I. H., "Graph Partitioning for Concurrent Test Scheduling in VLSI Circuit," *the 28th IEEE/ACM Design Automation Conference (DAC),* San Francisco, CA, pp. 287-290, June 1991.

121. Chen, C.-I. H. and Smith, R., "A Self-Testing and Self-Diagnostic Systolic Array Cell for Signal Processing," *the IEEE International Conference on Wafer Scale Integration*, San Francisco, CA, pp. 75-81, January 1991.

122. Chen, C.-I. H. and Sobelman, G., "Singleport/Multiport Memory Synthesis in Data Path Design," *the IEEE International Symposium on Circuits and Systems (ISCAS),* Portland, OR, pp. 1110-1113, May 1990.

123. Chen, C.-I. H., "A Top-Down Built-In Self-Test Design in VLSI Testing," *the IEEE International Symposium on Circuits and Systems (ISCAS),* Portland, OR, pp. 2720-2723, May 1990.

124. Chen, C.-I. H. and Smith, R., "Incorporating Self-Testing Capabilities into Systolic Array Cell for Digital Signal Processing," *the IEEE International Conference on Systems Engineering,* Pittsburgh, PA, pp. 240-243 August 1990.

125. Chen, C.-I. H.; Dixon, R.; Hohne, R.; Peterson, L. and Siferd, R., "Built-In Self Test and VLSI Stack-Frame Reduced Instruction Set Computer Architecture," *the IEEE National Aerospace and Electronics Conference*, Dayton, OH, pp. 130-132, May 1990.

126. Chen, C.-I. H., "An Implicit Acceleration Algorithm in Test Generation for VLSI Circuits," *the IEEE National Aerospace and Electronics Conference*, Dayton, OH, pp. 43-46, May 1990.

127. Chen, C.-I. H., "An Efficient Approach to Test Verification for VLSI Circuits", *the IEEE National Aerospace and Electronics Conference,* Dayton, OH, pp. 47-51, May 1990.

128. Chen, C.-I. H., etc. "Task Reallocation for Fault Tolerance in Multiprocessor Systems," *the IEEE National Aerospace and Electronics Conference*, Dayton, OH, pp. 495-500, May 1990.

129. Chen, C.-I. H., and Sobelman, G., "An Efficient Approach To Pseudo-Exhaustive Test Generation For BIST Design," *the IEEE International Conference on Computer Design (ICCD),* Boston, MA, pp. 576-579, October 1989.

RESEARCH GRANTS

Assured Digital Microelectronics Education & Training Ecosystem (ADMETE)
WSU proposal number 20-0191
Principal Investigator: Brian Rigling, $30M (7/1/2020 – 9/30/2023)
ADMETE team includes: WSU, U. of Acron, U. of Toledo, Ohio U., YSU, LCCC
Co-Investigator, my expenditure (**$107,758** (01/01/2020 – 12/31/2020); **$97,060** (01/01/2021 – 12/31/2021); **$70,424** (01/01/2022 – 12/31/2022))

Advanced Integrated Smart Cell Onboard Printed Electronics Development
Air Force Research Lab/DAGSI
Principal Investigator, **$218,706** (05/09/2016 - 12/31/2019)
($72,058 (05/09/2016 – 05/08/2017); $73,013 (05/09/2017 – 05/08/2018); $73,635 (05/07/2018 – 12/31/2019))

Non-Uniform Compressive Sensing Technique Development for EW Receiver Application
Air Force Research Lab/DAGSI
Principal Investigator, **$210,575** (05/06/2013 - 05/06/2016)
($69,360 (05/06/2013 – 05/05/2014); $70,521 (05/07/2014 – 05/06/2015); $70,694 (05/07/2015 – 05/06/2016))

Ultra High Chirp Rate Digital Chirp Receiver Using Monobit IFM Digital Receiver as a Core
Air Force Research Lab/DAGSI
Principal Investigator, **$203,754** (06/13/2011 - 06/12/2014)
($66,571 (06/13/11 – 06/12/12); $67,272 (06/13/2012 – 06/12/2013); $69,911 (06/13/2013 – 06/12/2014))

High Efficiency SIGINT Collection
EDAptive Computing, Inc
Principal Investigator, **$31,511** (11/07/2012 – 12/14/2013)

New Electronic Warfare Specialists Through Advanced Research by Students (NEWSTARS)
DoD, Air Force Research Lab, NEWSTARs Plus-Up
My expenditure for 2010: **$32,800** (01/01/2010 – 12/31/2010)

New Electronic Warfare Specialists Through Advanced Research by Students (NEWSTARS)
DoD, Air Force Research Lab, NEWSTARs Plus-Up
My expenditure for 2009: **$13,000** (01/01/2009 – 12/31/2009)

FPGA-Based High Instantaneous Two-Signal Dynamic Range Digital Wide-Band Microwave Receiver
DoD, AFRL and MacAulay-Brown, Inc. (MacB)
Principal Investigator, **$76,800** (04/10/2007 – 07/31/2008)

New Electronic Warfare Specialists Through Advanced Research by Students (NEWSTARS)
DoD, Air Force Research Lab, NEWSTARs Plus-Up
My expenditure for 2008: **$10,000** (01/01/2008 – 12/31/2008)

RoCSTARS: Receiver-on-Chip Signal Techniques and Reconfigurable Simulations
Systran Federal Corp.
Principal Investigator, **$1,140** (06/01/2006 – 03/31/2007)

New Electronic Warfare Specialists Through Advanced Research by Students (NEWSTARS)
DoD, Air Force Research Lab, NEWSTARs Plus-Up
My expenditure for 2007: **$50,517** (01/01/2007 – 12/31/2007)

Receiver and Processing Concepts Evaluation
DoD, Air Force Research Lab
My expenditure: **$67,980** (01/01/2005 – 12/31/2005)

New Electronic Warfare Specialists Through Advanced Research by Students (NEWSTARS)
DoD, Air Force Research Lab, NEWSTARs Plus-Up
My expenditure for 2006: **$59,160** (01/01/2006 – 12/31/2006)

Performance Improvement of a Receiver on a Chip
Systran Federal Corp.
Principal Investigator, **$15,000** (04/11/2005 – 01/10/2006)

Mathematic Model and Solution Approaches to the Systematic Design of Linear Feedback Shift Register (LFSR) BIST
The State of Ohio
Co-Principal Investigator, **$10,000** (06/01/2005 – 06/01/2006) (Co-PI: X. Zhang)

Receiver and Processing Concepts Evaluation
DoD, Air Force Research Lab,
My expenditure: **$53,650** (06/01/2004 – 12/31/2004)

Electronic Warfare (EW) Receiver-On-a-Chip (ROC)
DoD, Air Force Research Lab
Principal Investigator, **$300,000** (06/01/2003 – 06/01/2005) (Co-PI: Marty Emmert)

Timing Verification for High Speed CMOS Design Styles
Baynacre, Inc.
Principal Investigator, **$5,415** (05/1999 – 08/1999)

Complexity Management and Test/Diagnosis for Deep Submicron Integrated Circuit Design
State of Ohio
Principal Investigator, **$10,800** (01/01/1999 – 12/31/1999)

Automatic Vector Generation and False Path Verification in Static/Dynamic Timing Analysis
Baynacre, Inc. and ITRI
Principal Investigator, **$64,862** (08/01/1998 - 07/31/1999)

Optimal Physical Design, Design for Testability and Design Verification of a Monobit Receiver
DoD, Air Force Research Lab
Principal Investigator, **$25,350** (03/01/1998 – 08/30/1998)

A Coupling of Timing Analysis and Simulation for Deep Submicron Integrated Circuit (IC) Technology
Baynacre, Inc.
Principal Investigator, **$26,888** (12/01/1997 – 03/31/1998)

FFT Based VLSI Design Monobit Electronic Warfare Receiver
Air Force Office of Scientific Research (AFOSR)
Principal Investigator, **$100,000** (08/01/1996 – 03/31/1998)

Testable Circuit Design of an Enhancement Memory Chip (EMC)
Wright Laboratories of U.S. Air Force
Principal Investigator, **$20,000** (06/01/1996 – 12/31/1996)

VLSI Testability Synthesis on Graphics PIXEL VLSI Microcircuit
Wright Laboratories of US Air Force
Principal Investigator, **$25,000** (09/01/1995 - 05/15/1996)

VLSI Testability Synthesis Tool (VTST)
Wright Laboratories of US Air Force
Principal Investigator, **$547,148** (04/15/1993 - 05/15/1996)
($135,000 (04/1993 - 09/1994); $250,000 (09/1994 – 08/1995); $162,148 (09/1995 – 05/1996))

Internal Testability and Fault Coverage for MIPS R3x00
Texas Instruments
Principal Investigator, **$35,000** (11/1993 - 03/1994)

Using VHDL in VLSI BIST Synthesis and Its Application to 3-D PIXEL Graphics Chip
Air Force Office of Scientific Research (AFOSR)
Principal Investigator, **$20,000** (01/1993 - 12/1993)

VLSI VHDL Behavioral BIST Synthesis System
State of Ohio
Principal Investigator, **$21,435** (02/01/1993 - 12/31/1993)

A Study on Incorporating Built-In Self-Test (BIST) features into the MIPSCo R3000-derived microcircuits
LSI Logic Corporation
Principal Investigator, **$30,000** (06/01/1992 - 09/30/1992)

Modular Design Environment (MDE) Software System
LSI Logic Corporation
Principal Investigator, **$17,500** (06/01/1992 - 05/31/1993)

Advanced BIST Design on SF1 RISC Processor
State of Ohio
Principal Investigator, **$31,000** (01/01/1990 - 12/31/1991)

AWARDS and HONORS

Title of Award	**Granting Association**	**Dates**
Faculty Excellence in Outstanding	College of Engineering and Computer Science, WSU	2019
IEEE Harrell V. Noble Award	IEEE Dayton Section	2016
Nominee for Faculty Excellence in Research Award	College of Engineering and Computer Science, WSU	2015
Nominee for Faculty Excellence in Teaching Award	College of Engineering and Computer Science, WSU	2014
Nominee for Faculty Excellence in Teaching Award	College of Engineering and Computer Science, WSU	2007
Nominee for Faculty Excellence in Teaching Award	College of Engineering and Computer Science, WSU	2005
Faculty Excellence in Research Award	College of Engineering and Computer Science, WSU	1995

ACADEMIC SERVICE

CECS College Committees	**Position**	**Dates**
CECS Faculty Development Committee	Member	2021-present
CECS Steering Committee	Member	2018-present
CECS Dean Search Committee	Member	2019

CECS Associate Dean Search Committee	Member	2019
CECS Faculty Development Committee	Member	2018-2020
CECS Ad Hoc Committee for College Research Opportunities and Priorities		2018-2019
CECS Engineering Ph.D. Program Affairs Committee	Chair of Electronics, Microwave, VLSI, and Nanotechnology	2016-2020
CECS Faculty Development Committee	Member	2015-2017
CECS Engineering Ph.D. Student Affairs Committee	Chair of Electronics, Microwave, VLSI, and Nanotechnology	2015-2018
CECS Faculty Development Committee	Member	2014-2015
CECS Engineering Ph.D. Student Affairs Committee	Chair of Electronics, Microwave, VLSI, and Nanotechnology	2014-2015
EE Department Chair Search Committee	Member	2013-2014
CECS Scholarship Committee	Member	2013-1014
CECS Scholarship Committee	Chair	2011-2012
CECS Scholarship Committee	Member	2010-2011
CECS Student Affair Committee	Chair	2009-2010
CECS Student Affair Committee	Member	2008-2009
CECS Academic Computing Committee	Member	2008-2009
CECS Engineering Ph.D. Student Affairs Committee	Chair of Electronics, Microwave, VLSI, and Nanotechnology	2008-2010
CECS Engineering Ph.D. Student Affairs Committee	Chair of Electronics, Microwave, VLSI, and Nanotechnology	2007-2008
EE Department Chair Search Committee	Member	2007-2008
CECS Ph.D. Student Affairs Committee	Chair of Microwave and Electronics	2006-2007
EE Department Chair 5-year Review Committee	Member	2006-2007
CECS Graduate Council Standing Committee	Member	2005-2006
CECS Engineering Ph.D. Student Affairs Committee	Chair of Microwave and Electronics	2005-2006
CECS Engineering Ph.D. Student Affairs Committee	Chair of Microwave and Electronics	2004-2005
CECS Engineering Ph.D. Program Committee	Member	1996-2004
CECS Faculty Development Committee	Member	2003-2005
CECS Library Committee	Chair	2003-2004
CECS Due Process	Member	2003-2004
CECS Library Committee	Chair	2002-2003
CECS Ad Hoc General Education Committee	Member	2000-2003
CECS Ad Hoc Bylaws Review Committee	Member	1998-1999
CECS Petitions Committee	Chair	1998-1999
CECS Petitions Committee	Member	1997-1998
CECS Academic Mediations Committee	Member	1994-1996
CECS Dayton Area Graduate Studies Institute	Member	1992-1993

Department Committees	**Position**	**Dates**
Ad Hoc Student Affairs Committee	Member	2016-present
Faculty Development Committee	Member	2009-present
Graduate Study Committee	Member	2009-present
Faculty/Instructor Search Committee	Chair	2014-2015
Instructor Search Committee	Chair	2011-2012
Laboratory Resources Committee	Member	2009-2012
Faculty Search Committee	Chair	2009-2010
Laboratory Resources Committee	Chair	2008-2009
Electronic/VLSI Subcommittee	Chair	2006-2008
Faculty Development Committee	Chair	2004-2005
Faculty Development Committee	Member	2000-2009
Faculty Search Committee	Member	1999-2009
Undergraduate Studies Committee	Member	2004-2008
Undergraduate Studies Committee	Chair	2003-2004
Electronic/VLSI Subcommittee	Chair	2003-2004
Graduate Studies Committee	Member	2003-2009

Laboratory Resources Committee	Member	2003-2009
Department Bylaw Committee	Member	2005-2007
Ad Hoc: Department Bylaw Committee	Member	2000-2003
Graduate Studies Committee	Member	1996-1999
Graduate Studies Committee	Member	1992-1993
Undergraduate Petitions Committee	Chair	1997-1999
Undergraduate Petitions Committee	Member	1994-1997
Laboratory Development Committee	Member	1989-2000
Curriculum Subcommittee for Electronics	Member	1990-2001

COURSES TAUGHT Graduate (G) and Undergraduate (U)

EE8000 - Tools Mixed Signals (G)
EE7510 - Digital Wideband Receiver Design (G)
EE7520 - Low Power VLSI System Design (G)
EE7530 - VLSI Design Synthesis and Optimization (G)
EE7540 - VLSI Testing and Design for Testability (G)
EE7580 - CMOS Analog Circuit Design (G)
EE4620 - Digital Integrated Circuit Design with PLDs and FPGAs (U&G)
EE4540 - VLSI Design (U&G)
EE4440 - Electronic Integrated Systems (U&G)
EE3310 - Electronic Devices and Circuits (U)
EE2000 - Digital Design with VHDL (U)

Visiting Scholar

Chunjie Zhang	Associate Professor, College of Information and Communication Engineering, Harbin Engineering University, China (11/2015 -11/2016)
Wenxu Zhang	Lecturer, College of Information and Communication Engineering, Harbin Engineering University, China (4/2017- 4/2018)

Ph.D. DISSERTATION SUPERVISED

Continuing Students

Kiran Jayarama	High Two-Signal Dynamic Range Digital Wideband Receiver for Multiple Signal Detection: Theory, Design, and System Integration (date passed Ph.D. Candidacy Exam: Summer 2019, Ph.D. Proposal Defense: Fall 2023)
Bilal Abdulhamed	Deep Learning for Chirp Signal Detection and Classification in Digital Wideband Receivers: Theory, Design, and System Integration (date-passed Ph.D. Candidacy Exam: Spring 2023)
Prasanna Kumar Daram	Smart Fast Fourier Transform: Algorithm, Application, and Implementation, (date passed Ph.D. Candidacy Exam: Spring 2016)
Feiran Liu	High Two-Signal Dynamic Range and Accurate Frequency Measurement Wide-band Digital Receiver: Theory, Design and System Integration (date passed Ph.D. Candidacy Exam: Fall 2016)

Graduated Students

Jianfeng Ren	CMOS Wide Tuning Inductor/Inductorless Gilbert Mixer with Controllable Bandwidth for Multi-Band/Multi-Standard Applications in Upcoming RF Frontends Fall 2023 (initial employer: China Southern Power Grid, Guangzhou, China)
Yu Wang	Design and Implementation of Fully Integrated CMOS On-chip Bandpass Filter with Wideband High-Gain Low Noise Amplifier, Summer 2021 (initial employer: Qualcomm, San Diego, CA)
Jian Chen	RF CMOS Band Pass Filters with Wide Tuning Frequency, Controllable Pass Band and High Stopband Rejection: Using Passive and Active Inductors, Fall

	2016 (initial employer: Assistant Professor, Dongguan University of Technology, Donguan, China)
Ethan Lin	Compressed Sensing for Electronic Radio Frequency Receiver: Detection, Sensitivity, and Implementation, Dec. 2015 (Riverside Research, Dayton, OH)
Stephen Benson	Modern Digital Chirp Receiver: Theory, Design and System Integration, Dec. 2015 (Raytheon, Tucson, AZ)
George Y.-H. Lee	Dynamic Kernel Function Fast Fourier Transform Variable Truncation Error Analysis and Performance Evaluation, Dec. 2009 (Northrop Grumman, Dayton, OH)
Kumar Yelamarthi	Process Variation Aware Timing Optimization with Load Balance of Multiple Paths in Dynamic and Mixed-Static-Dynamic CMOS Logic, June 2008 (Full Professor of Electrical Engineering, Central Michigan University, Mount Pleasant, MI)
Mingzhen Wang	High-Speed Low-Power Pipelined Flash A/D Converter for System-on-a-Chip Applications, Dec. 2007 (initial employer: Assistant Professor of Electronic Engineering Department at University of Electronic Science and Technology of China, Chengdu, China)
Kiran George	Design and Performance Evaluation of 1 Giga Hertz Wideband Digital Receiver, Sept. 2007 (Full Professor of Computer Engineering, California State University, Fullerton, CA)

M.S. THESES SUPERVISED

Graduated Students

Priscilla Sharon Allwin	A Low-Area Energy-Efficient 64-Bit Reconfigurable Carry Select Modified Tree Based Adder for Multimedia Signal Processing, Summer 2019 (continue Ph.D. in the Eindhoven University of Technology, Netherlands)
Akshay A. Rajendraprasad	High-Speed Testable Radix-2 N-Bit Signed-Digit Adder, Summer 2019 (Intel, Portland, Oregon)
Bilal Abdulhamed	Digital Instantaneous Frequency Measurement Receiver for and Fine frequency and High Sensitivity, Spring 2019 (Ph.D at Wright State University)
Praneeth Namara	A 13T Single-Ended Low Power SRAM Using Schmitt-Trigger and Write-Assist, summer 2017 (initial employer: Micron Technology Inc., Allen, Texas)
Xin Hu	RF CMOS Tunable Gilbert Mixer with Wide Tuning Frequency and Controllable Bandwidth: Design Synthesis and Verification, spring 2017
Yu Wang	Tunable Coupled-Capacitor Band Pass Filter with Resonators Using Active Capacitor and Inductor, summer 2016 (Continue Ph.D. at Wright State University)
Lihzong He	1-GHz CMOS Analog Signal Squaring Circuit, summer 2016
Feiran Liu	High Resolution and Dynamic Range Adaptive Thresholding Wideband Digital Receiver, Dec. 2015 (Ph.D at Wright State University)
Julin Sha	Compressive Sensing Analog Front-End Design in 180 nm CMOS Technology, Summer 2015 (initial employer: Nishtech, Cincinnati, OH)
Surya Kiran Akkaladevi	Design and Performance Analysis of Magnetic Adder and 16-Bit MRAM Using Magnetic Tunnel Junction Transistor, Spring 2015 (employer: Cerner Corporation, Kansas City, Missouri)
Linda Chu	Adaptive I/Q Mismatch Compensation for Wideband Receiver, fall 2014 (initial employer: Riverside Research, Dayton, OH)
Kaushik Katpally	Dynamic Repeater with Booster Enhancement for Fast Switching Speed and Propagation in Long Interconnect, fall 2014 (initial employer: OmniPHY Semicondutor in Hyderabad, India)
Hao Xue	Timing and Power Optimization for Mixed-Dynamic-Static CMOS, summer 2013 (Intel, Portland, Oregon)
Duo Zhang	Dynamic CMOS MIMO Circuits with Feedback Inverter Loop and Pull-Down Bridge, summer 2013
Ramadan Buzukuk	Dynamic Footed with Clock Overlapping and Load Balancing in Multiple Paths for Noise Tolerance in Dynamic CMOS Circuits, fall 2011 (initial employer: Qualcomm, San Diego, CA)

A. Vaidyanadeswaran	Circuit Techniques on Improving Timing and Noise in Dynamic CMOS, winter 2011 (initial employer: Intel, Folsom, CA)
Stephen Benson	Adaptive Thresholding for Detection of Radar Receiver Signals, summer 2010 (continue Ph.D. at Wright State University)
Dilip S. Murthy	Real-Time Hilbert Transform and Auto-correlation for Digital Instantaneous Frequency Measurement Receiver, fall 2008 (initial employer: IBM India Pvt Ltd, India)
Ryan Bone	FPGA-Based Low-Power 256-point FFT Processor, estimated summer 2008 (initial employer: Science Applications International Corporation (SAIC), Beavercreek, OH)
Vivek Sarathy	High Spurious-Free Dynamic Range Digital Wideband Receiver for Multiple Signal Detection and Tracking, fall 2007 (initial employer: QuStream Corportion, Huntsville, AL)
Rajasekhar Keerthi	Stability and Static Noise Margin Analysis of Static Random Access Memory, fall 2007
James Helton	FPGA-Based Processor for Digital Instantaneous Frequency Measurement (IFM) Receiver, summer 2007 (initial employer: Science Applications International Corporation (SAIC), Beavercreek, OH)
Brian Poling	On-Chip Signal Generation and Response Waveform Extraction for Analog Built-In Self-Test of General Receiver Systems, summer 2007 (WPAFB, Dayton, OH)
Tony Chiang	Design and Performance Evaluation of a Discrete Wavelet Transform Based Multi-Signal Receiver, spring 2006 (initial employer: Daetwyler Corp., Dayton, OH)
Cyprian Sajabi	FPGA Frequency Domain Based GPS Code Acquisition Processor Using FFT, spring 2006 (initial employer: Nova Systems Solutions, Cincinnati, OH)
Siaw-Yuen Ng	Automated Generation, Optimization and Synthesis of 2-Dimensional Linear Feedback Shift Registers Framework for Built-In Self-Test, spring 2006 (initial employer: Jiin & Associates Co. Ltd., Segamat, Johor, Malaysia)
Sashank Kakulavarapu	High Speed Signed Multiplier Using Baugh-Wooley & On-The-Fly Conversion Algorithms, winter 2005 (initial employer: Harvard Pilgrim, Boston, MA)
Vivek Chandrasekhar	Low-Cost Low-Power Self-Test Design and Verification for On-chip ADC in System-on-a-Chip Applications, winter 2005 (initial employer: Intel Corp., Folsom, CA)
Jason Wibbenmeyer	Built-In Self-Test for Low-Voltage High-Speed Analog-to-Digital Converters, winter 2005 (initial employer: Ameren, St. Louis, MO)
Soumya Ramaswamy	High Speed 64-bit Thermometric Square-Root Carry Select Adder Based on the Chinese Abacus, winter 2005
Rathod Snehal	Architecture of Hybrid Signed-Digit Adder using Carry-Free Property of Redundant Arithmetic and Parallel Redundant-to-Binary Converter, winter 2005
Shailesh Radhakrishnan	A Low-Power 4-b 2.5 Gsample/s Flash Analog-to-Digital Converter Using QV Comparator and DCVSPG Encoder, fall 2004 (initial employer: Link Electronics, Cape Girardeau, Missouri)
Darren Schindel	Arc Draw Algorithm Utilizing Bresenham Circle Algorithm and Multiple Clipping Techniques For Graphics Generation Using an Active Matrix Liquid Crystal Display, fall 2004 (initial employer: Unisys, Polymouth, MI.)
Kumar Yelamarthi	Design Synthesis of Re-Convergent Manchester Carry Chain Adders, fall 2004 (continue Ph.D. at Wright State University)
Nilesh Gunjal	Design Synthesis of High-Speed Testable Hybrid Adders, fall 2004 (initial employer: Cingular Wireless, Dallas, TX)
Pavan Lingamaneni	Low-Power Low-Leakage Asymmetric SRAM using Dual Threshold Voltages, summer 2004
Mahesh Subramanian	Pipeline with Scan Insertion for Timing Driven Testable Convergent Tree Adders, summer 1999 (initial employer: Intel Corporation, San Jose, CA)
N. Thiagarajan	VHDL Modeling, Simulation and Synthesis of Fully-Testable Fast Binary Carry-Save Multiplier without Final Addition, summer 1998 (initial employer: NEC America, Austin, TX)
Mahesh Wagh	High-Level Design Synthesis with Redundancy Removal for High Speed Testable Binary Adders, summer 1998 (initial employer: Intel Corporation, Seattle, WA)

Khalil Habash	VHDL Modeling, Simulation and Testing of a Fast Binary Adder with Conditional Carry Generator, summer 1997 (initial employer: Cray Research Corporation, Wisconsin)
Joaquin Romera	Timing-Driven Testable VLSI Parallel Adders, summer1997 (initial employer: Intel Corporation, Portland, OR)
Rajesh Palamadai	Implementation of Dynamic Huffman Coding Using CAM-Based CMOS VLSI Architecture, winter 1997 (initial employer: Mentor Graphics, Warren, NJ)
Sin Kwang Pok	High Level Test Generation and Test Verification for the Enhanced Memory Chip (EMC), summer 1996 (initial employer: Baynacre, Union City, CA)
Anil Kempanna	Cellular Automata Based Test Generator, winter 1995 (initial employer: Cadence Spectrum Design, San Diego, CA)
Anup Kumar	Area-Time Optimal Digital Mixed CMOS/BiCMOS Parallel Adders, winter 1995 (initial employer: Credence Systems Corporation, Fremont, CA)
Chia-Lin Chan	Efficient Methods for Partial Scan Sequential Circuit Design, fall 1994 (initial employer: Oak Technology, Sunnyvale, CA)
Tim Noh	VHDL Behavioral Fault Modeling and Fault Simulation System, April 1994 (initial employer: FORE Systems, Inc., Warrendale, PA)
Vijay K. Singh	Circular Built-In Self-Test in VLSI Circuits, fall 1993 (initial employer: Advanced Micro Devices, Austin, TX)
Joel Yuen	Concurrent Testing and VLSI Built-In Self-Test Design in Systolic Array Chip, fall 1992 (initial employer: Intel Corp., Chandler, AZ)
Ji-Der Lee	Testability Enhancement and Hardware Partition for Testable Design, spring 1992