RAYMOND E. SIFERD

Department of Electrical Engineering
Wright State University
Dayton, OH 45435

Phone: 937-775-5058 Fax: 937-775-3936
Email: Ray.Siferd@wright.edu

EDUCATION

Institution	Concentration	Degree/Date
Air Force Institute of Technology	Electrical Engineering	Ph.D. 1977
Air Force Institute of Technology	Astronautical Engineering	M.S. 1965
University of New Mexico	Electrical Engineering	M.S. 1963
Ohio State University	Electrical Engineering	B.E.E. 1959

ACADEMIC EXPERIENCE

Institution	Position	Dates
Wright State University	Emeritus Professor	09/99-present
Wright State University	Chair, Dept. of Electrical Engineering	08/92-08/99
Wright State University	Professor	09/96-08/99
Wright State University	Associate Professor	09/86-08/96
Wright State University	Assistant Professor	09/81-08/86

OTHER PROFESSIONAL EXPERIENCE

Institution	Position	Dates
Wright Patterson AFB, OH Avionics Laboratory	Chief Systems Avionics Division	06/78-08/81
Wright Patterson AFB, OH Foreign Technology Division	Chief Directed Energy System Division	08/74-07/77
Air Force Studies and Analysis HQ USAF, Pentagon, Washington, DC	Systems Analyst	08/69-07/72
Directorate of Nuclear Safety Kirtland AFB, New Mexico	Electrical Engineer	09/65-07/69
Air Force Weapons Laboratory Kirtland, AFB, New Mexico	Electrical Engineer	08/59-08/63
General Motors Technical Center Warren, MI	Electrical Engineer	06/59-07/59

PROFESSIONAL MEMBERSHIPS

Association	Status	Dates
Institute of Electrical & Electronics Engineers (IEEE)	Member	1973-Present
Tau Beta Pi	Member	1957-Present
Eta Kappa Nu	Member	1957-Present
Phi Eta Sigma	Member	1955-Present

PROFESSIONAL AWARDS

Title of Award	Granting Association	Dates
IEEE Student Chapter Teaching Excellence Award	Wright State University	1985-1986
College of Engineering & CS Outstanding Faculty Award	College of Engineering and CS Wright State University	1988-1989
College of Engineering & CS, Nominee for WSU Faculty Teaching Excellence Award	College of Engineering and CS Wright State University	1988-1989
1999 Outstanding Engineers & Scientists Award	Affiliates Societies Council of Dayton	1999
Harrell V. Noble Award for R&D in Electronics	Dayton Section of IEEE	2004

PRINTED SCHOLARSHIP

Articles

1. Boon Cheah, Saiyu Ren, Ray Siferd, "Design Algorithm and Hardware Implementation of FIR Compensation Filter Implemented in 0.13um CMOS Technology", WSEAS Transactions on Circuits and Systems, Issue 12, Vol 4, pages 1421-1433, December 2005.
2. K. H. Abed and R. E. Siferd, "CMOS VLSI Implementation of a Low Power Logarithmic Converter", IEEE Transactions on Computers, Vol 52, pages 1421-1433, November 2003
3. K. H. Abed and R. E. Siferd, "VLSI Implementation of a Low Power Antilogarithmic Converter", IEEE Transactions on Computers Vol52, pages 1221-1228, September 2003.
4. Rong Wang, Ray Siferd, Robert Ewing, "CMOS Analog Implementation of a Discrete Time 9 Tap FIR Filter with Circular Buffer Architecture", Journal of Analog Integrated Circuits and Signal Processing, Vol 28, Pages 149-159, 2001.
5. Xu, Jing; Siferd, Ray; Ewing, Robert, "High Performance CMOS Analog Arithmetic Circuits", Journal of VLSI, Signal Processing Systems for Signals, Image, and Video Technology, Vol. 22, No. 2, September 1999. (Joint Special Issue on Mixed Signal Design)
6. Xu, Jing; Siferd, Ray; Ewing, Robert, "High Performance CMOS Analog Arithmetic Circuits", Journal of Analog Integrated Circuits and Signal Processing, Vol. 20, No. 3, September 1999. (Joint Special Issue on Mixed Signal Design)
7. Gomez, G. and Siferd, R. E., "An Adaptive Noise Canceler Implemented with CMOS Analog Technology," *Journal of Circuits, Systems and Computers*, special issue on Hardware Implemented Neural Networks, Vol. 6, No. 2, pp. 139-154, 1996.
8. Cravens, R. C.; Siferd, R. E. and Kazimierczuk, M. K., "CMOS PWM Control Circuit with Programmable Dead Time," *Journal of Circuits*, *Systems and Computers*, special issue on Power Electronics, Vol. 5, No. 3, pp. 429-441, 1995.
9. Siferd, R. E., "A GaAs Four Quadrant Analog Multiplier Circuit," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 3, pp. 388-392, March 1993.
10. Shanbhag, N. R, and Siferd, R. E. "A Single Chip Pipelined 2-D FIR Filter Using Residue Arithmetic," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 5, pp. 796-805, May 1991.
11. Shanbhag, N. R.; Nagchoudhuri, D.; Siferd, R. E. and Visweswaran, G.S., "Quaternary Logic Circuits in 2 Micron CMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 3., pp. 790-799, June 1990.
12. Longway, C. and Siferd, R., "A Doughnut Layout Style for Improved Switching Speed with CMOS VLSI Gates," *IEEE Journal of Solid-State Circuits*, Vol. 24, Issue 1, pp. 194-198, February 1989.
13. Longway, C.; Siferd, R. E. and Dixon, R. D., "A VLSI Implementation of a Stack-Frame Computer," *The Journal of Forth, Applications and Research*, Vol. 5, No. 1, pp. 165-168, 1987.
14. Siferd, Raymond E., "Pipelined VLSI Systolic Array and Algorithm for Digital Filtering," *International Journal of Mini and Microcomputers*, Vol. 9, No. 1, pp. 20-23, 1987.

U. S. Patents

1. Ray Siferd and Saiyu Ren, “Pipelined Delta Sigma Modulator Analog to Digital Converter”, Provisional Patent Application, April 25, 2006.
2. Ray Siferd, “Parallel Time Interleaved Delta Sigma Modulator”, February 11, 2003.

Papers Published in Full and Official Proceedings

1. Saiyu Ren, Ray Siferd, Robert Blumgold, Nima Emami, “Pipelined Delta Sigma Moduator Analog to Digital Converter, IEEE Midwest Circuits and Systems Symposium, San Juan, P.R., August, 2006.
2. David Rodney and Ray Siferd, “Digital Channelized Wideband Receiver Implemented with Systolic Array of Multirate FIR Filters” , IEEE Midwest Circuits and Systems Symposium, San Juan, P.R., August, 2006.
3. Saiyu Ren, Ray Siferd, Robert Blumgold, “Hardware Efficient FIR Compensation Filter for Delta Sigma Analog to Digital Converters” IEEE Midwest Circuits and Systems Symposium , Cincinnati, OH, August, 2005.
4. Michael Myers and Ray Siferd, “PLL with Fuzzy Logic Nonlinear Gain Controller”, IEEE Midwest Circuits and Systems Symposium , Cincinnati, OH, August, 2005.
5. Saiyu Ren, Ray Siferd, and Robert Blumgold, “Parallel Time Interleaved Delta Sigma Band Pass Analog to Digital Converter for SOC Applications”, IEEE International System on Chip Conference, Santa Clara, CA, September, 2004
6. Michael Myers, Saiyu Ren, Mingzhen Wang, and Ray Siferd “Broadband Delta Sigma Modulator with 1 GHz Sampling Rate and 4 Bit Quantizer in 0.18um CMOS Technology” NASA Symposium on VLSI Design, Coeur d’Alene, Idaho, May, 2003
7. Vivek Venugopal, Khalid Abed, Raymond Siferd, and Shailesh Nerurkar, “Hardware Efficient Narrow Band FIR Filter,” IEEE International Midwest Symposium on Circuits and Systems, Tulsa, Oklahoma, August 4-7, 2002, pp. 223-226.
8. Shailesh Nerurkar, Khalid Abed, Raymond Siferd and Vivek Venugopal, “Low Power Sigma Delta Decimation Filter,” IEEE International Midwest Symposium on Circuits and Systems, Tulsa, Oklahoma, August 4-7, 2002, pp. 647-650.
9. Siferd, R.; Ren, S.; Grimes, T.; Blumgold, R.; Cerny, C.; Chang, T. “100 MHz Delta Sigma Modulator with 4-Bit Quantizer in 0.35um CMOS Technology” The 2002 International Multiconference in Computer Science, VLSI ‘ 02, Las Vegas, Nevada, June, 2002.
10. Abed, K.; Siferd, R.; “CMOS VLSI Implementation of 16-Bit Logarithm and Anti-logarithm Converters”, IEEE Midwest Symposium on Circuits and Systems, Detroit, Michigan, August, 2000.
11. SanGregory, Samuel, L.; Siferd, Raymond E., and Brothers, Charles, “A Fast, Low-Power Logarithm with CMOS VLSI Implementation”, IEEE Midwest Symposium on Circuits and Systems, Las Cruces, NM, August 1999.
12. Wei, J.; Qian, X.; and Siferd, R. “CMOS Implementation and Performance of β-Bit Serial/Parallel Multipliers,” IEEE Midwest Symposium on Circuits and Systems, Las Cruces, NM, August 1999.
13. Balakrishnanan, V.; Ramaswamy, S.; and Siferd, R., “Fast/Area Efficient 8-Bit A/D and D/A Designs in 0.8 Micron CMOS Technology Using Layout Generators”, *IEEE National Aerospace and Electronics Conference*, Dayton, OH, July 1997 (best student paper)
14. Loonawat, G. and Siferd, R. E., “FPGA Implementation of a FIR Filter Using Residue Arithmetic”, Proceedings of the *IEEE National Aerospace and Electronics Conference*, Dayton, OH, May 1996.
15. Ramaswamy, S. and Siferd, R., “CMOS VLSI Implementation of a Digital Logarithmic Multiplier”, Proceedings of the *IEEE National Aerospace and Electronics Conference*, Dayton, OH, May 1996.
16. Moogat, F. and Siferd, R., “A 60 MHz ASIC for β-Bit Serial/Parallel Multiplier,” *Proceedings of the IEEE ASIC Conference*, Rochester, NY, pp. 458-462, September 1994.

17. Sathi, P. and Siferd, R., “Pipelined 50 MHz CMOS ASIC for 32 Bit Binary to Residue Conversion and Residue to Binary Conversion,” *Proceedings of the IEEE ASIC Conference*, Rochester, NY, pp. 454-458, September 1994.

18. Cravens, R. C.; Siferd, R. E. and Kazimierczuk, M. K., “CMOS Design of PWM Control Circuitry for Power Converters,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH, May 1994.

19. Mahurin, E. and Siferd, R., “Sigma-Delta Modulator and Decimation Filter Using GaAs Technology,” *Proceedings of the 1993 IEEE Application Specific Integrated Circuit (ASIC) Conference*, Rochester, NY, pp. 15-18, September 1993.

20. Malholtra, R. and Siferd, R. E., “Evaluations and Comparisons of Electronic Artificial Neural Network Implementations,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH, pp. 885-891, May 1993.

21. Shetty-Wagoner, M.; Rattan, K. and Siferd, R., “Membership Function Generator Circuit for a Fuzzy Logic Controller,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH, pp. 48-53, May 1993.

22. Siferd, R. E.; Permumal, S. and McCormick, W. “A CMOS ASIC for Real Time Microwave Spectral Estimation Applications,” *Proceedings of the IEEE ASIC 92 Conference*, Rochester, NY, pp. 68-72, September 1992.

23. Yuen, J.; Chen, C. H. and Siferd, R., “VLSI Design and Implementation of a Self Testing Systolic Array Chip for Signal Processing,” *Proceedings of the 1992 IEEE International Symposium on Circuits and Systems*, San Diego, CA, pp. 375-378, May 1992.

24. Siferd, R., “A Monolithic Four Quadrant Analog Multiplier Circuit in Gallium Arsenide Technology,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH, pp. 101-107, May 1992.

25. Gomez, G. and Siferd, R., “Single Chip FIR Adaptive Filter Using CMOS Analog Circuits,” *Proceedings of the IEEE ASIC 91 Conference*, Rochester, NY, pp. P3-5.1-P3-5.5, September 1991.

26. DaWalt, S.; Ossa, L.; Siferd, R. and Yeazel, S., “A 20 MHz Low Power CMOS ASIC for a 1553 Bus Interface Unit,” *Proceedings of the IEEE ASIC 91 Conference*, Rochester, NY, pp. P4-22.1-P4-2.5, September 1991.

27. Gomez, G. and Siferd, R., “A Sampled-Data CMOS Analog Adaptive Filter,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH, Vol. 1, pp. 106-111, May 1991.

28. Shanbhag, N. R. and Siferd, R. E., “A Pipelined Systolic 2-D FIR Filter Using Residue Arithmetic,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH, Vol. 1, pp. 98-101, May 1990.

29. Chen, C. H.; Dixon, R. D.; Hohne, R.; Peterson, L. and Siferd, R., “Built-in Self Test and VLSI Stack-Frame Reduced Instruction Set Computer Architecture,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH, Vol. 1, pp. 130-133, May 1990.

30. Jundi, K. and Siferd, R. E., “Sampled Data Analog Signal Processor,” *IEEE National Aerospace and Electronics Conference*, Dayton, OH, Vol. 1, pp. 64-67, May 1990.

31. Hohne, Robert and Siferd, R., “A Programmable High Performance Processor Using the Residue Number System and CMOS VLSI Technology,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH, Vol. 1, pp. 41-44, May 1989.

32. Spalding, George R., Jr. and Siferd, Raymond E., “A Monolithic CMOS Phase-Locked Loop Capable of Operating with Low Signal to Noise Ratios,” *Proceedings of the Colorado Microelectronic Conference*, Colorado Springs, CO, p. 37-61, March 1989.

33. Dixon, R. D.; Calle, M.; Longway, C.; Peterson, L. and Siferd R., “The SF1 Real Time Computer,” Proceedings of the IEEE National Aerospace and Electronics Conference, Dayton, OH, Vol. 1, pp. 60-64, May 1988.

34. Sweet, Francis W. and Siferd, Raymond E., “Design of a Programmable Digital Filter using CMOS VLSI Technology,” *Proceedings of the 5th International Symposium on Systems Engineering*, Dayton, OH, pp. 457-460, September 1987.

35. Siferd, R. E., “Design and Performance of a Custom VLSI Array Processor for Linear Phase Transversal Filtering,” *Proceedings of the IASTED International Symposium on Applied Control*, Filtering, and Signal Processing, Geneva, Switzerland, pp. 73-77, June 1987.

36. Peterson, L. S.; Dixon, R. D. and Siferd, R. E., “Design of a VLSI 32-Bit Word-Addressable Hardware Stack for a Stack-Frame Microprocessor,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH, Vol. 1, pp. 14-19, May 1987.

37. Birbal, J. V. and Siferd, R. E., “Performance of Custom VLSI Circuit for Programmable Signal Processing,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH Vol. 1, pp. 9-13, May 1986.

38. Siferd, R. E. and Maybeck, P. S., “Sufficient Conditions for Establishing Maximum Likelihood Estimates for Nonlinear Process Parameters,” *Proceedings of the 24th IEEE Conference on Decision and Control*, Ft. Lauderdale, FL, Vol. 1, pp. 212-214, December 1985.

39. Siferd, R. E., “Pipelined VLSI Systolic Array,” *Proceedings of the ISMM Symposium on Mini and Microcomputers and their Applications*, Montreal, Canada, pp. 48-51, June 1985.

40. Siferd, R. E., “Pipelining Highly Concurrent VLSI Processors to Meet Stringent Finite Impulse Filter Requirements,” *Proceedings of the IEEE National Aerospace and Electronics Conference*, Dayton, OH, Vol. 1, pp. 2-7, May 1985.

41. Siferd, R. E. and Brandeberry, J. E., “VLSI Implementation of a Fully Digital Transversal Filter,” *Proceedings of the IEEE National Aerospace and Electronic Conference*, Dayton, OH, Vol. 1, pp. 14-19, May 1984.

42. Brandeberry, J.; Rattan, K.; Siferd, R. and Spalding, G., “Inexpensive Teaching Robot,” *Proceedings of the 2nd Annual Workshop on Interactive Computing: CAD/CAM,* Electrical Engineering Education, pp. 147-151, November 1983.

43. Brandeberry, J. E.; Rattan, K. S. and Siferd, R. E., “Design and Implementation of Servo-control for a Robotic Arm,” *Proceedings of the IEEE National Aerospace and Electronic Conference,* Dayton, OH, Vol. 1, pp. 189-196, May 1983.

44. Siferd, R. E. and Maybeck, P. S., “Stochastic Identifiability of Nonlinear Dynamical System Parameters,” *Proceedings of the 14th Annual Modeling and Simulation Conference*, University of Pittsburgh, Vol. 14, pp. 343-348, April 1983.

45. Siferd, R. E. and Maybeck, P. S., “Identifiability of Nonlinear Dynamical Systems,” *Proceedings of the 21st IEEE Conference on Decision and Control*, Orlando, FL, Vol. 3, pp. 1167-1171, December 1982.

46. Siferd, R. E. and Maybeck, P. S., “Identifiability of Nonlinear Dynamical Systems with an Application to the Optimal Control Model for the Human Operator,” *Proceedings of the 13th Annual Modeling and Simulation Conference*, University of Pittsburgh, Vol. 13, pp. 243-248, April 1982.

47. Siferd, R. E., “Computer Architecture Standardization,” *Proceedings of the AFSC Standardization Conference*, Dayton, OH, Vol. 1, pp. 1-10, November 1980.

RESEARCH CONTRACTS AND GRANTS

1. “Advanced CMOS IF Receiver Stage, Phase II”, Raytheon RF Components, Jan 2007-Sept 2007, Principal Investigator, $60,000

2. “Advanced CMOS IF Receiver Stage, Phase I”, Raytheon RF Components, December 2005-December 2006, Principal Investigator, $102,000

3. “High Speed Read Out Integrated Circuit for IR Focal Plane Array Phase II”, RNET Technologies, April 2006-April 2008, Principal Investigator, $300,000

4. “High Speed Read Out Integrated Circuit for IR Focal Plane Array Phase I”, RNET Technologies, May 2005-Dec 2005, Principal Investigator,$33,000

5. “Wideband Array Analog to Digital Converter”, Systran Federal Corporation, June 2004-June2007, Principal Investigator,$330,000.

6. “Reconfigurable Architectures for Tactical Radio Systems”, University of Dayton Research Institute, May 2004-May 2005, Principal Investigator,$62,000.

7. “Parallel Time Interleaved Pipelined Delta Sigma Analog to Digital Converter”, Systran Federal Corporation, May 2003-Oct 2005, Principal Investigator,$300,000.

8. “High Speed/Resolution Delta Sigma Analog to Digital Converter”, Systran Federal Corporation, May 2001-May 2003, Principal Investigator,$353,000.

9. “Parallel Sub-sampling Analog to Digital Converter” Systran Federal Corporation, June 2002-March 2003, Principal Investigator,$33,000.

10. “Radiation Hardened Analog to Digital Converter, Systran Federal Corporation”, April 2001-January 2002, Principal Investigator,$33,000.

11. “Analog to Digital Converter Development”, Systran Federal Corporation, April 2001-January 2002, Principal Investigator,$33,000.

12. “CMOS Analog Adaptive Filter”, University of Cincinnati, January 1, 1999 – December 31, 2000, Principal Investigator,$47,000.

13. “CMOS Analog Adaptive Filter”, University of Cincinnati, January 1, 1999 – December 31, 1999, Principal Investigator,$47,000

14. “Mechatronic Design Environment”, University of Cincinnati, June 15, 1999-September 15, 1999, Principal Investigator,$4,497

15. “Design Library Function Generator”, Wright Laboratories, Wright Patterson AFB, OH, March 28, 1997 – June 1999, Principal Investigator, $40,000.

16. “CMOS Submicron Cell Generators”, Wright Laboratories, Wright Patterson AFB, OH, September 29, 1995 - June 30, 1997, Principal Investigator, $40,000.

17. “CMOS Digital Function Cell Generators,” Wright Laboratories, Electronics Directorate, Wright Patterson AFB, OH, June 15, 1995-September 29, 1995, Principal Investigator, $19,582.

18. “Ohio Micro-electromechanical Systems (MEMS) Net,” Ohio Board of Regents Investment Fund, July 1995, with Case Western Reserve (lead), Ohio State, University of Cincinnati, University of Toledo, co-Principal Investigator, $2,400,000 total, $100,000 WSU.

19. “Fabrication of VLSI Circuits for Class Projects,” National Science Foundation, MOSIS, September 1994-September 1995, $5600.

20. "C-HFET Digital Function Cell Generators,” Wright Laboratories, Electronics Directorate, Wright Patterson AFB, OH, June 1994-May 1995, Principal Investigator, $17,390.

21. Educational Grant, Xilinx, Development Tools for Field Programmable Gate Arrays, Xilinx Corporation, February 1993, $15,350. Tools used for new course on Programmable Logic Devices and Field Programmable Gate Arrays.

22. “Fabrication of VLSI Circuits for Class Projects,” National Science Foundation, MOSIS, September 1993-September 1994, $5700.

23. “Fabrication of VLSI Circuits for Class Projects,” NSF, MOSIS, September 1992-September 1993, $6730.

24. “Design and Simulation of Gallium-Arsenide Second-Order Sigma-Delta Analog to Digital Converter,” Electronics Directorate, Wright Patterson AFB, OH, January 1993-June 1993, Principal Investigator, $17,500.

25. “GaAs Sigma Delta Modulator,” Electronic Laboratory, Wright Patterson AFB, OH, June 1992-December 1992, Principal Investigator, $17,310.

26. “Fabrication of VLSI Circuits for Class Projects,” National Science Foundation; MOSIS, September 1991-September 1992, $4,950.

27. “Fabrication for VLSI Circuits for Class Projects,” National Science Foundation, September 1990-September 1991, $11,618.

28. “Microelectronic Implementation of Computer Bus Interface Unit,” Ohio Edison Program with Digital Technology, Inc., September 1990-September 1991, Principal Investigator, $45,654

29. “Microelectronic Implementation of a Computer Bus Interface Unit,” Digital Technology, Inc., September 1990-September 1991, Principal Investigator, $18,678.

30. “Fabrication of VLSI Circuits for Class Projects,” National Science Foundation, September 1989-September 1990, $10,000.

31. “Advanced 32-Bit Stack Architecture with Built-in Self Test,” WRDC, Wright Patterson AFB, OH August 1989-August 1991, Principal Investigator, $249,105.

32. “A VLSI Array Compiler System,” Co-investigator with J. S. Jean, National Science Foundation, August 1989-June 1991, $24, 815. This effort focused on the development of CAD tools for designing systolic/wavefront arrays.

33. “Fabrication of VLSI Circuits for Class Projects,” National Science Foundation, September 1988-September 1989, $16,000.

34. “Avionics Integration, Southeastern Center for Electrical Engineering Education (SCEEE), March 1988-August 1988, Principal Investigator, $23,897.

35. Educational Grant for NCR Standard Cell VLSI Software, NCR Corporation, Dayton, OH, September 1987, $14,000 estimated initial value.

36. “Advanced 32-Bit Stack Architecture,” AFWAL, Wright Patterson AFB, OH, September 1987-January 1990, Principal Investigator, with R. D. Dixon, Senior Investigator, $296,954.

37. “Student Task-Avionics Integration,” Southeastern Center for Electrical Engineering Education (SCEEE), June 1987 to June 1988, $4900

38. “Fabrication of VLSI Circuits for Class Projects,” National Science Foundation, July 1987-June 1988, $29,200.

39. “Educational Grant for Mentor Graphics Software for VLSI Design using Apollo Workstation and NCR Cell Libraries,” May 6, 1987, $204,000 estimated initial value (support continues).

40. Addition to Integrated Circuits for Avionics,” AFWAL, Wright Patterson AFB, OH, May 1987. Additional funds custom VLSI effort, Principal Investigator, $44,000.

41. “VLSI Hardware System Design Using Standard Cell Libraries and Silicon Compilers,” Ohio Research Challenge, January-December 1987, Principal Investigator, with R. D. Dixon and A. D. McAulay, $50,000.

42. “Custom VLSI Circuit for Signal Processing,” Ohio Research Challenge, June 1986-August 1987, Principal Investigator, $34,000.

43. “Maintenance and Fabrication Costs, Integrated Circuits for Avionics,” AFWAL, Wright Patterson AFB, OH, February 1986-June 1989; Funds a portion of VLSI system maintenance and fabrication costs, Principal Investigator, $35,000.

44. “DOD Sponsored VLSI Fabrication Service for Educational Purposes,” NSF, August 1985-June 1987, Principal Investigator. Fabrication of VLSI chips for education, $20,000.

45. “DOD Sponsored VLSI Fabrication Service for Research Purposes,” DARPA, Washington, DC, August 1985, Principal Investigator. Fabrication of VLSI Chips for research projects, 2 years, $50,000.

46. “Integrated Circuits for Avionics,” AFWAL, Wright Patterson AFB, OH, June 1985-June 1989, Principal Investigator, $196,000.

47. “Preliminary Design of a Custom VLSI Circuit,” RADC Contract F30602-81-C-0206, August-September 1984, Principal Investigator, $5400.

48. “A Robot for Robotic System Research,” seed grant with G. S. Spalding, 1983, $2850.

TECHNICAL REPORTS

Chaudhry, S., and Siferd, R., “C-HFET Digital Function Cell Generators,” Final Report, Wright Laboratory, Contract F 33615-92-C-2056, August 1995.

Mahurin, E., and Siferd, R., “Design and Simulation of a Gallium-Arsenide Second-Order Sigma-Delta Analog-to-Digital Converter,” Final Report, Wright Laboratory Contract F33615-92-C-1056, August 1993, 63 pages.

Mahurin, E., and Siferd, R. E., “GaAs Sigma Delta Modulator,” Final Technical Report, Electronics Directorate Contract, December 1992.

Siferd, R. E., Peterson, L., Hohne, R., Dixon, R., Calle, M., Longway, C., Krieder, J., Hanselman, P., “Advanced 32-Bit Stack Processor Architecture,” WL-TR-91-1057 Volumes I-IX, Final Report, September 1991.

Siferd, R. E., Ossa, L., Dawalt, S., Yeazel, S., “Microelectronics Implementation of a Computer Bus Interface Unit,” Final Technical Report, Edison Project #202, October 1991.

Siferd, R. E., “Integrated Circuits for Avionics,” WRDC-TR-89-1118, Final Report, October 1989, 113 pages.

Siferd, R. E., “Preliminary Design of a Custom VLSI Circuit for a Programmable Bandpass Filter,” Final Report, RADC Contract F30602-81-C-0206, October 1984, 31 pages.

Siferd, R. E., “An Algorithm for Predicting Detection of Ships in Sea Clutter by Airborne Radar,” Final Report, Studies and Analysis, Pentagon, Washington, D.C., April 1972.

Siferd, R. E., “Bomber Penetration of Terminal Defenses,” Final Report, Studies and Analysis, Pentagon, Washington, D.C., February 1972.

INVITED LECTURES

“Custom VLSI Circuits for Signal and Data Processing,” Invited Lecture, University of Toledo, Department of Electrical Engineering Symposium, May 1987.

“Digital Avionics Information System, and the Air Force Acquisition Management,” AIAA Electronic Systems Acquisition Management Conference, Washington, D.C., April 1979.

“Low Altitude Penetration of Surface-to-Air Missile Defenses,” President of the U.S. Scientific Advisory Committee, La Jolla, CA, August 1971.

M.S. THESES SUPERVISED

1.	J. V. Birbal	“Design of a Programmable Digital Filter Using NMOS VLSI Components,” December 1986
2.	F. W. Sweet	“Design of a Programmable Digital Filter Using CMOS VLSI Technology,” December 1987
3.	M. Calle	“VLSI Implementation of a 32-bit ALU for the SF-1 Computer,” March 1988
4.	C. Longway	“Instruction Sequencing and Decoding in the SF-1,” March 1988
5.	G. Spalding	“A Monolithic CMOS Phase Lock Loop Capable of Tracking Signals Corrupted by Noise,” August 1988
6.	J. Stauffer	“A PC/AT Interface to the SF-1 Computer,” December 1988
7.	R. Hohne	“A High Performance Vector Processor Using Residue Number Theory, Pipelining, and VLSI Technology,” June 1989

8. M. Swaminathan "Toeplitz Eigen System Solver Using Systolic Architecture," July 1989
9. R. Ram "A 2-Dimensional Convolution Chip," July 1989
10. J. Fernando "VLSI Implementation of Fast Integer Multiply and Divide Algorithms," September 1989
11. K. Jundi "CMOS Analog Integrated Circuit Library," September 1989
12. T. Quinn "Design of a Multiplier-Accumulator Array Using Modular CMOS VLSI Components," December 1989
13. J. Kreider "Hardware Prototype for SF-1 Computer," March 1990
14. N. Shanbhag "Design and Implementation of a Pipelined Single Chip Two Dimensional Finite Impulse Response Filter Using Residue Arithmetic," August 1990
15. P. Hanselman "Alternative Instruction Set Architectures for a Stack Frame RISC Computer," June 1990
16. W. Teal "SFI Overflow Stack Addressing with Linear Feedback Shift Registers," December 1990
17. G. Gomez "CMOS VLSI Implementation of a Discrete-Time Analog Adaptive Filter," March 1991
18. L. Peterson "The Stack-Frame Processor Architecture and SFI and SF2000 VLSI Implementations," April 1991
19. L. Ossa "CMOS VLSI Implementation of a 1553 Bus Interface Unit," September 1991
20. S. Dawalt "The Conversion of an Existing 1553 Bus Product into a CMOS ASIC," December 1991
21. R. Grewe "Design and Implementation of a High Level Language Computer System," August 1992
22. R. Neff "Bi CMOS Standard Cells," December 1992
23. T. Dermis "Sigma-Delta Analog to Digital Converter Using CMOS Technology," June 1993
24. J. Meyers "A VHDL Register Transfer Level Model of the Linear Token Passing Multiplex Data Bus Protocol," June 1993
25. E. Mahurin "Sigma-Delta Analog to Digital Converter Using GaAs Technology," June 1993
26. M. Chaudhry "Design of Silicon VLSI/Ferroelectric Liquid Crystal Optoelectronic Computing Devices," June 1993
27. S. Perumal "Design and Implementation of a Pipelined 32 Bit Binary to Residue and Residue to Binary Converters," April 1994
28. D. Williams "Design of High Speed Data Cache Using Gallium Arsenide Technology," August 1994
29. F. Moogat "VLSI Implementation of β-Bit Serial/Parallel Multiplier," June 1994
30. S. Chaudhry "Digital Function Cell Generators Using CHFET Technology," August 1995
31. E. Khan "Unique Architecture for VLSI Implementation of a Finite Impulse Response Filter", December 1995
32. D. Shaffer "A VLSI Implementation of a Microprocessor for Real-Time Systems," March 1996
33. G. Loonawat "FPGA Implementation of an Adaptive Filter Using Residue Arithmetic," March 1996
34. S. Ramaswamy "Digital Function Cell Generators Using Sub-micron CMOS Technology," December 1996
35. V. Balakrishnan "Macro-Gel Generators Using Submicron CMOS Technology," June 1997
36. J. Daniel "VLSI Architecture for a Median Filter," June 1997
37. I. Abraham "Continuously Variable MEMS Capacitor MEMS," December 1997
38. S. Haddad "CMOS Analog to Digital Converter," December 1998
39. B. McKanna "Low Power FIR Filter," March 1998
40. B. Werst "A 19 Bit CMOS Floating Point Newton Raphson Divider," June 1998
41. R. Kumar "Resonance in MEMS Cantilever," August 1998
42. X. Qian "Serial/Parallel Multipliers," June 1999
43. G. Pujara "CMOS Sigma Delta A/D Converter," June 1999
44. A. Kazimierczuk "CMOS ASIC for Sensor Data Storage," June 1999
45. Rong Wang " CMOS Analog Implementation of a Discrete Time 9 Tap FIR Filter with Circular Buffer Architecture" Mar 2000
46. Gopal Iyer "FPGA Implementation of a 9 Tap Adaptive FIR Filter" Apr 2000
47. Anessa Kunju "An FPGA Implementation of a 2D Pipelined Median Filter" Apr 2000
48. Hailing Ding "Alternative Architectures for Oversampling Sigma Delta Analog to Digital Converters" Sept 2000

49. Saiyu Ren "Integrated Circuit Design of Delta Sigma Moulators Using The MIT Lincoln Laboratory 0.25um Fully Depleted CMOS Silicon Insulator Proces May 2001
50. Michael Myers "The Design and Comparison of Two Sigma Delta Modulators" Jul 2002
51. Terrence Powell "Silicon Germanium S-Band Low Noise Amplifier" Dec 2002
52. Boris Holowko "Self Repair Based on the Method of Modular Redundancy for Programmable Devices" Mar 2003
53. Miguel Gomez "Time Interleaved Analog to Digital Converters" Mar 2004
54. Ramya Ramachandran, "Wide Range Low Power Phase Locked Loop" Dec 2004
55. Boon Cheah "Compensation Filter for Analog to Digital Converter in 130 nM CMOS Technology" Dec 2005
56. Ryan McGinnis "Flexible Analog to Digital Converter Architectures for Advanced Receivers" June, 2006
57. Matt Gerald "Direct Digital Frequency Synthesizer" June 2006
58. David Rodney "Channelized RF Receiver in CMOS Technology " June 2006
59. Kumar Subramany "Design and Performance Assessment of Low Power CMOS PLL Frequency Synthesizer", March 2006
60. Banty Jain "Design and Implementation of a CMOS Direct Digital Frequency Synthesizer" March 2006
61. Rohit Chakraborty, "FPGA Design and Implementation of a Phase Shift Key Receiver", June 2006

Ph.D. THESES SUPERVISED

1. Jian Wei "Improving Channel Transmission Quality for Telecommunications by Oversampling and Adaptive Filtering", Completed All but Dissertation.
2. Khalid Abed "VLSI Implementation of Logarithm and Anti-Logarithm", December 2000.
3. Michael Myers "Clock Generation and Distribution on Microelectronic Circuits", In Progress
4. Saiyu Ren "High Performance Analog to Digital Converters", In Progress

TEACHING AWARDS

1988-1989	College of Engineering and Computer Science Outstanding Faculty Award
1988-1989	College of Engineering and Computer Science Nominee for University Teaching Excellence Award
1985-1986	IEEE Student Chapter Teaching Excellence Award

SERVICE

COMMITTEE SERVICE

University Committees	Position	Dates
Wright State University Quality Council	Member	1997-1998
DAGSI Research Coordinator Committee	Member	1996-present
Research and Doctoral Programs Committee, Ohio Board of Deans	Member	1996-1997
Education Committee, OAI	Member	1993-1994
Academic Council	Member	1992-1994
Graduate Council	Member	1991-1993
WSU Planning Council	Member	1990-1993
Tenure Removal Committee	Member	1989-1992
Budget Review Committee	Member	1989-1990
Academic Council	Member	1988-1989
Steering Committee	Member	1988-1989
Academic Council	Member	1987-1988
Steering Committee	Member	1987-1988

College Committees		
Dept. of Biomedical & Human Factors, Chair Search Committee	Chair	1996, 1997
Faculty Development Committee (Promotion & Tenure)	Member	1995-1996
Steering Committee	Member	1995-1996

Advising Committee for NSF Engineering Research Center Proposal	Member	1994-1995
Dept. of EE Search Committee for Chair	Member	1994-1995
Ad Hoc Committee on Assessment	Member	1994-1995
Steering Committee	Member	1994-1995
Faculty Development Committee (Promotion & Tenure)	Member	1994-1995
Department of Computer Science Search Committee for Chair	Member	1993-1994
Faculty Workload Committee	Member	1993-1994
Faculty Development Committee (Promotion & Tenure)	Member	1993-1994
Faculty Committee, Dayton Area Graduate Studies Institute	Member	1993-1993
Steering Committee	Member	1993-1994
Steering Committee	Chair	1992-1993
Dayton Area Graduate Studies Institute	Faculty Committee	1992-1993
Faculty Development Committee (Promotion & Tenure)	Member	1992-1993
Steering Committee	Chair	1991-1992
Ad Hoc Committee on Graduate Education and Research	Member	1990-1991
5 Year Review Committee for Dean, College of E&CS	Member	1990-1991
Steering Committee	Member	1990-1991
Faculty Development Committee (Promotion & Tenure)	Member	1989-1990
Research Challenge Review Committee	Member	1989-1990
3 Year Administrative Review Committee for Dean, Clg of E & CS	Member	1988-1989
Faculty Development Committee (Promotion & Tenure)	Member	1988-1989
Ad Hoc Committee for Review of Electronics Shop	Chair	1987-1988
Research Challenge Review Committee	Member	1987-1988
Faculty Development Committee (Promotion & Tenure)	Member	1987-1988
Search Committee for Computer Science Dept. Chair	Member	1987-1988
Faculty Development Committee (Promotion & Tenure)	Member	1986-1987
Search Committee for Electrical Engineering Department Chair	Member	1985-1986
Academic Mediation Committee	Chair	1984-1985
Academic Mediation Committee	Member	1983-1984

Department Committees	**Position**	**Dates**
Curriculum Committee	Member	1998
Engineering Physics Program Committee	Member	1998
Engineering Physics Program Committee	Member	1995-1996
Curriculum Committee	Member	1994-1995
Engineering Physics Program Committee	Member	1994-1995
Engineering Physics Program Committee	Member	1993-1994
Curriculum Committee	Member	1993-1994
Curriculum Committee	Member	1992-1993
Awards Committee	Member	1991-1992
Lab Development Committee	Member	1992-1993
Curriculum Committee	Member	1990-1991
5 Year Review Committee for Chair, Department of EE	Member	1990-1991
Faculty Recruitment Committee	Chair	1989-1990
Curriculum Committee	Member	1989-1990
Faculty Recruitment Committee	Member	1989-1990
Curriculum Committee	Member	1988-1989
Faculty Recruitment Committee	Member	1987-1988
Curriculum Committee	Member	1987-1988
Curriculum Committee	Chair	1986-1987
Faculty Recruitment Committee	Member	1986-1987
Search Committees for Mechanical & Electrical faculty positions	Member	1983-1985

Other Committees	**Position**	**Dates**
Wright State University Student Chapter of IEEE	Faculty Advisor	1987-1990
WSU Chapter of Tau Beta Pi (Electrical Engineering)	Faculty Advisor	1985-present
Tutorial Sessions, 1990 IEEE NAECON Conference, Dayton OH	Chair	1989-1990

VLSI System Design Session of Ohio Collegiate CS Conference	Chair	1989
Control Systems Society Dayton Section of IEEE	Chair	1983-1984
Control Systems Society Dayton Section of IEEE	Secretary	1982-1983
Steering Committee of Engnrng Mmnt Soc, Dayton Section of IEEE	WSU Representative	1982-1984
Presented Tutorial Session on “Introduction to Robotics” with Drs. Brandeberry and Rattan, Spalding at NAECON ‘83	Member	1983
IEEE Transactions on Circuits and Systems	Reviewer	

SUMMARY OF TEACHING

EE 431	Electronic Circuits
EE 434	Electronic Circuits Laboratory
EE 441	Electronic Circuits
EE 449	Pulse and Digital Circuits
EE 454	VLSI Design
EE 752	VLSI I
EE 753	VLSI II
EE 758	CMOS Analog Integrated Circuit Design
EE 759	RF CMOS Analog Integrated Circuit Design