



## Graduate Research Assistant (GRA) Opportunity

While Intel is investing \$20 billion to build a factory in Ohio to host “Intel 18A” process and CHIPS and Science ACT is signed recently by the President, it’s time to join the exciting research of microelectronic devices! This is a three-year project at AFRL. Tuition and stipend will be fully covered. Yearly stipend increase is guaranteed. To qualify this project, the student must be a U.S. citizen and could be a newly started graduate student or an undergraduate student who’s in 4+1 program or interested in pursuing graduate degree next Fall. If you are interested in this opportunity, please contact with Dr. Weisong Wang, [weisong.wang@wright.edu](mailto:weisong.wang@wright.edu)

### Project description:

Successful integration of dielectrics into a transistor process flow with negligible defect density has historically been the key for wide scale application of electronic devices. Dielectrics are needed not only as gate insulators for operation of metal oxide semiconductor field-effect transistors (MOSFETs), they are also needed for passivation of metal semiconductor FET (MESFET) and high-electron mobility transistors (HEMT; which is a different form of MESFET). The presence of defects either in the bulk or in the interface of these dielectrics critically affects the performance of transistors. Transistors for RF operation use all the above transistor configurations. The semiconducting channel in these transistors are generally made with III-V (like GaAs, GaN, AlGaIn) or III-O (like Ga<sub>2</sub>O<sub>3</sub>, AlGaO) materials. These materials do not have a native dielectric as Si has in the form of SiO<sub>2</sub>; and therefore, have an unoptimized dielectric/semiconductor interface even 40 years after their introduction into RF electronics. In addition, formation of novel dielectrics on these materials poses additional challenges in terms of bulk and interface defects, and carrier injection into dielectric, which leads to instability in device operation. Significant research opportunities therefore exist in integrating classical and novel dielectrics in III-V and III-O based semiconductors. These are especially important for high power RF applications that require use of wide bandgap (WBG) materials like III-N and III-O and require high voltage application across the dielectric.

This research targets successful integration of dielectrics in high-power GaN-based RF transistors. This will require optimization of a wide range of process parameters during device fabrication in AFRL/RY’s class 100 (ISO-5) cleanroom. Resultant devices will go through extensive electrical (C-V, I-V, transient, noise), optical (different forms of spectroscopy and microscopy) and materials characterization for confirming the effect of different process parameters on device performance.

